INTEGRATED TECHNICAL EDUCATION CLUSTER
AT ALAMEERIA

J-601-1448
Electronic Principals

Lecture #5
FET Biasing & AC Analysis

Instructor:

Dr. Ahmad El-Banna

NOVEMBER 2014

Agenda

Note!
Same concepts of the BJT, so we will just overview the FET transistors.

- Construction and Characteristics
- FET Biasing
- Design and Troubleshooting
- JFET small signal Model
- FET Amplifier Networks
- Practical Applications

CONSTRUCTION AND CHARACTERISTICS

Construction

- One of the most important characteristics of the FET is its high input impedance.
- FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

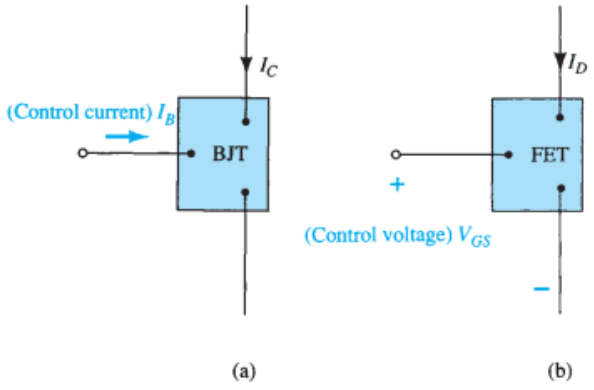


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

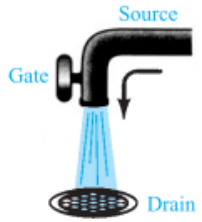


FIG. 6.4
Water analogy for the JFET control mechanism.

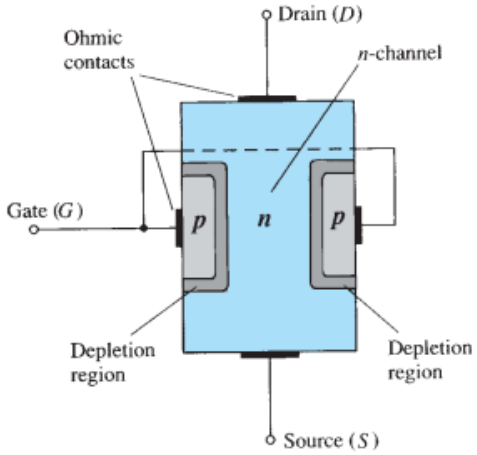


FIG. 6.3
Junction field-effect transistor (JFET).

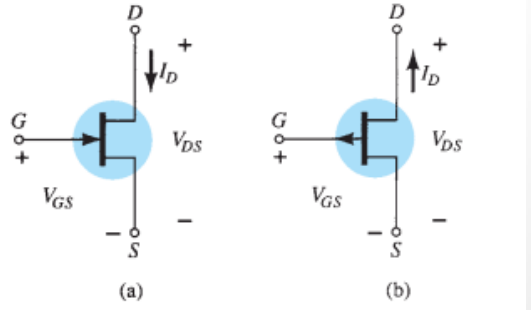


FIG. 6.14
JFET symbols: (a) n-channel; (b) p-channel.

Construction..

N-channel

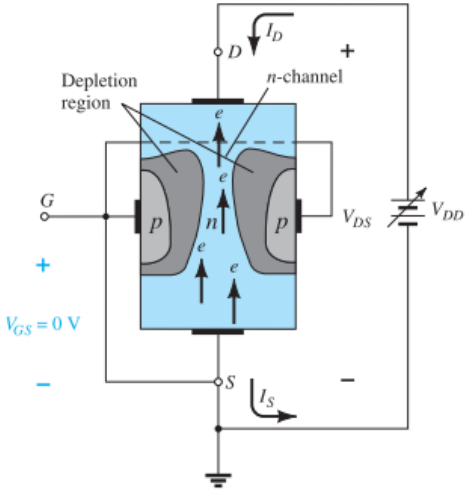


FIG. 6.5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

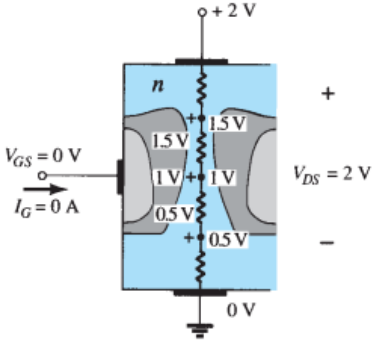


FIG. 6.6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

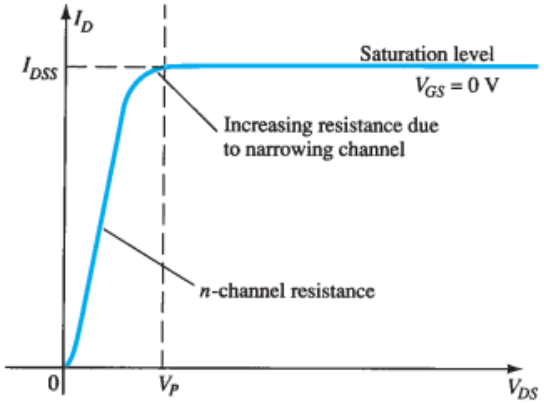


FIG. 6.7
I_D versus V_{DS} for $V_{GS} = 0$ V.

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

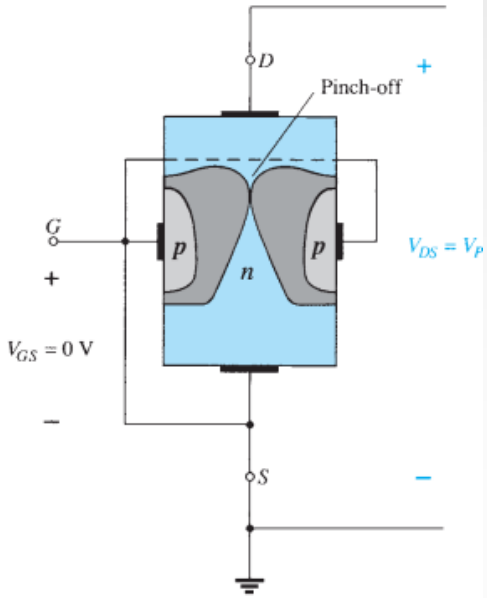


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

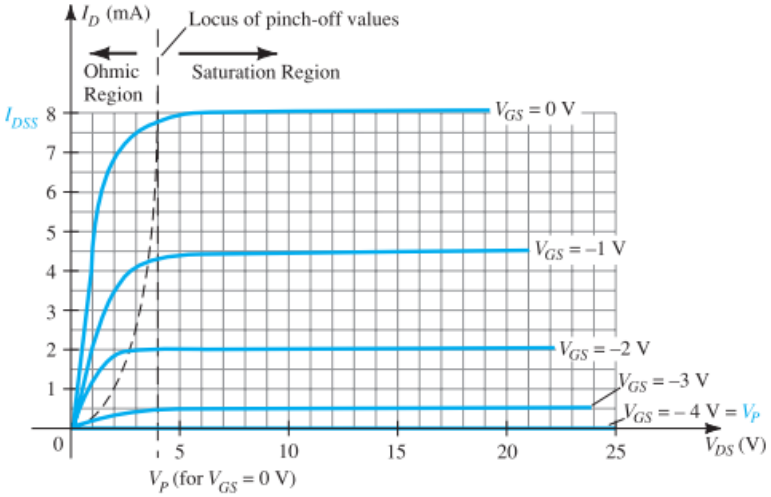


FIG. 6.11
n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

Characteristics & Equations

control variable

$$I_C = f(I_B) = \beta I_B$$

constant

control variable

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

constants

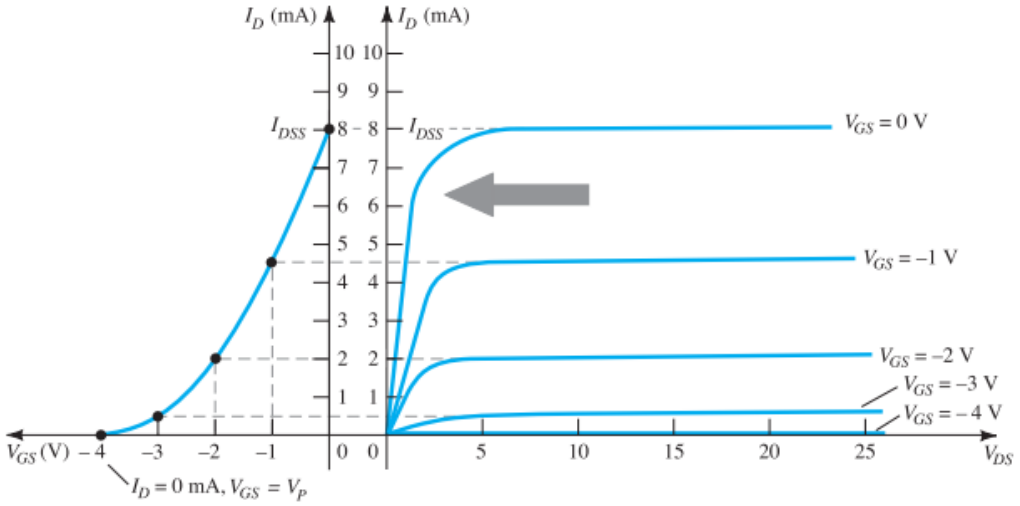


FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

TABLE 6.2

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

When $V_{GS} = 0$ V, $I_D = I_{DSS}$

When $V_{GS} = V_P$, $I_D = 0$ mA

$$I_D = I_{DSS}\,|_{V_{GS}=0\,V}$$

$$I_D = 0\,A\,|_{V_{GS}=V_P}$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS} I_D$$

Depletion-Type MOSFET

- There is no direct electrical connection between the gate terminal and the channel of a MOSFET.
- It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

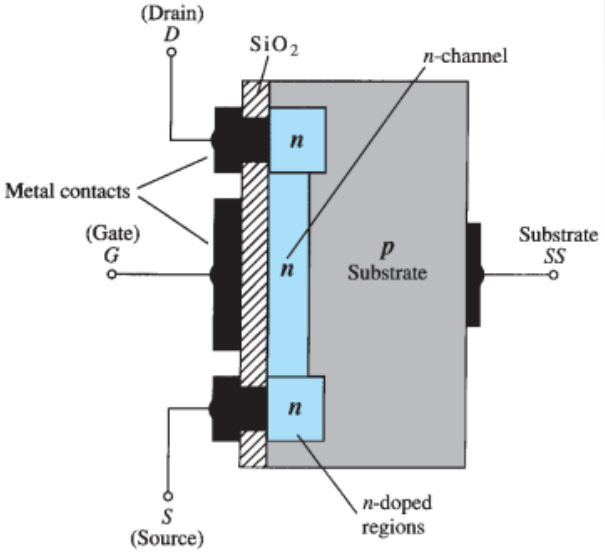


FIG. 6.24
n-Channel depletion-type MOSFET.

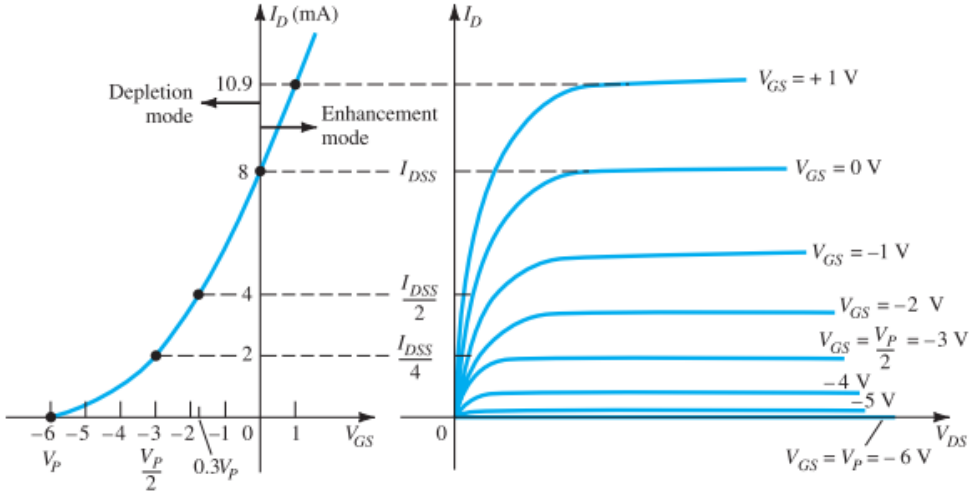


FIG. 6.26
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

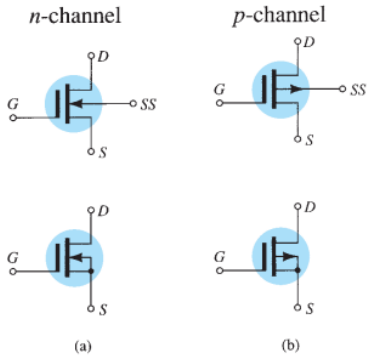


FIG. 6.30
Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.

Depletion-Type MOSFET

$$V_{DG} = V_{DS} - V_{GS}$$

$$V_{DS_{sat}} = V_{GS} - V_T$$

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

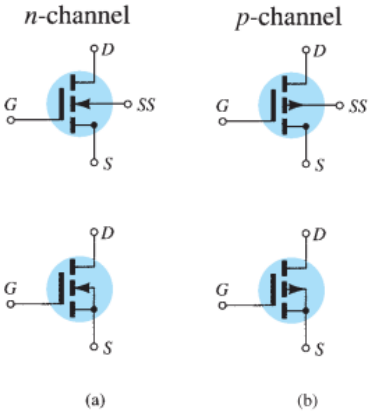


FIG. 6.39
Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.

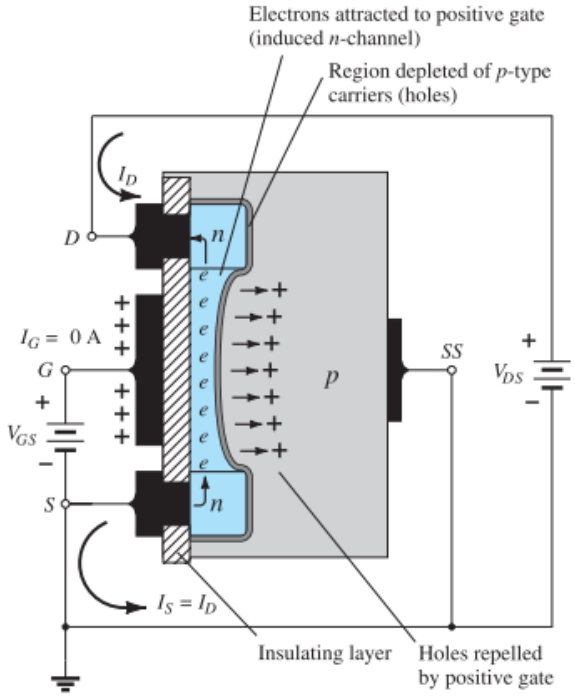


FIG. 6.33
Channel formation in the n-channel enhancement-type MOSFET.

Other MOSFETS

- VMOS AND UMOS POWER MOSFETs

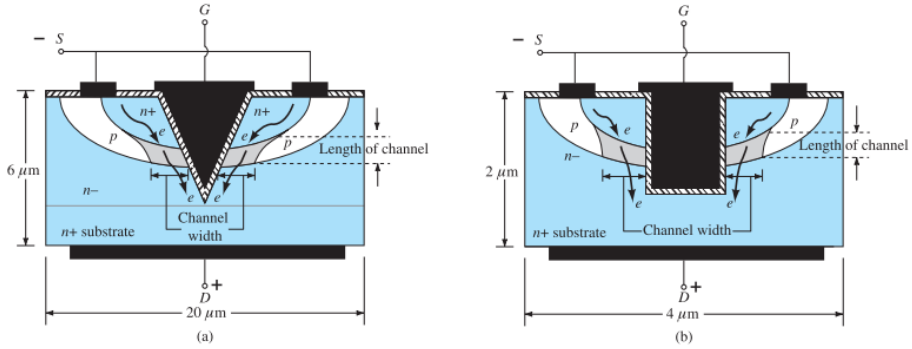


FIG. 6.43
(a) VMOS MOSFET; (b) UMOS MOSFET.

- CMOS

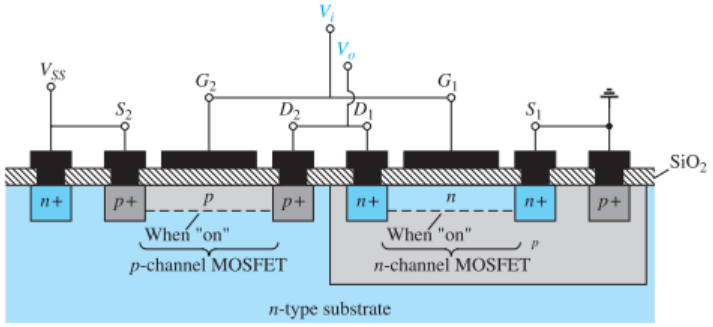


FIG. 6.44
CMOS with the connections indicated in Fig. 6.45.

- MESFET

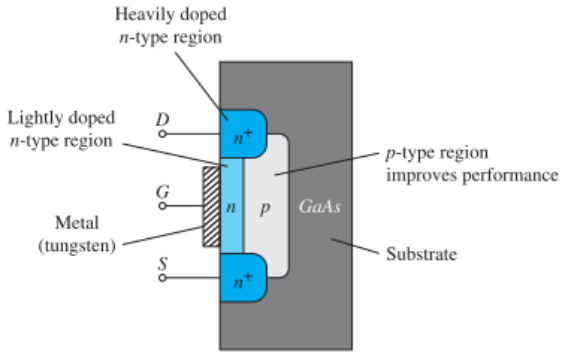


FIG. 6.47
Basic construction of an n-channel MESFET.

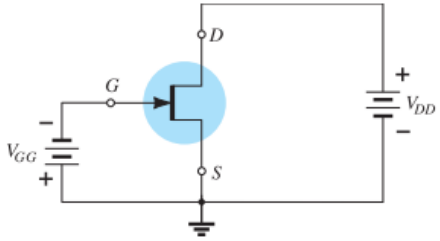


FIG. 6.49
Symbol and basic biasing arrangement for an n-channel MESFET.

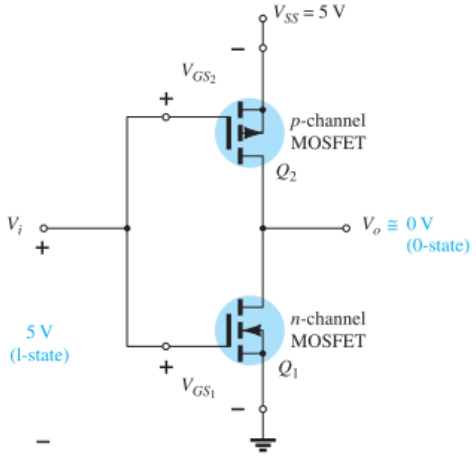


FIG. 6.45
CMOS inverter.

FET BIASING

FIXED-BIAS CONFIGURATION

$$I_G \cong 0\ \text{A}$$
$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$

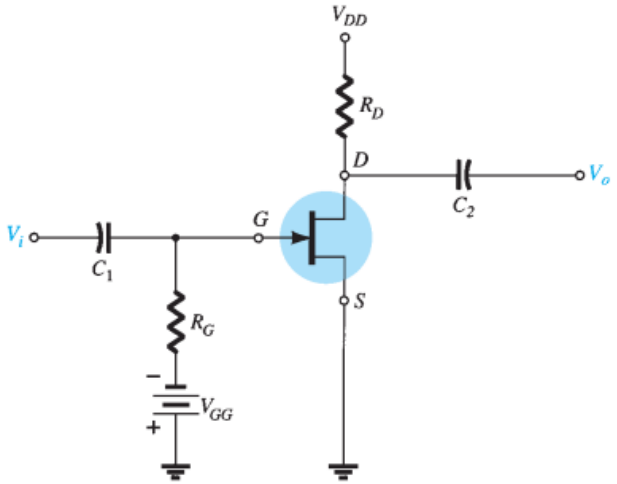
$$-V_{GG} - V_{GS} = 0$$
$$\boxed{V_{GS} = -V_{GG}}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

$$\boxed{V_S = 0\ \text{V}}$$



$$V_{DS} = V_D - V_S$$
$$V_D = V_{DS} + V_S = V_{DS} + 0\ \text{V}$$

$$\boxed{V_D = V_{DS}}$$

$$V_{GS} = V_G - V_S$$
$$V_G = V_{GS} + V_S = V_{GS} + 0\ \text{V}$$

$$\boxed{V_G = V_{GS}}$$

Example

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

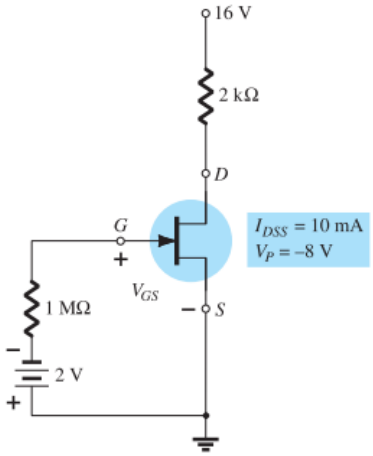


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

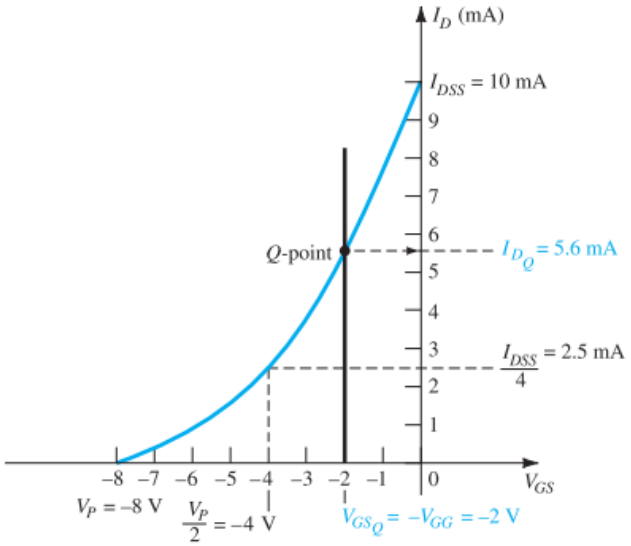


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\ V}$$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

Voltage-Divider Bias

$I_G \cong 0\ \text{A}$

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_G - V_{GS} - V_{R_S} = 0$$
$$V_{GS} = V_G - V_{R_S}$$

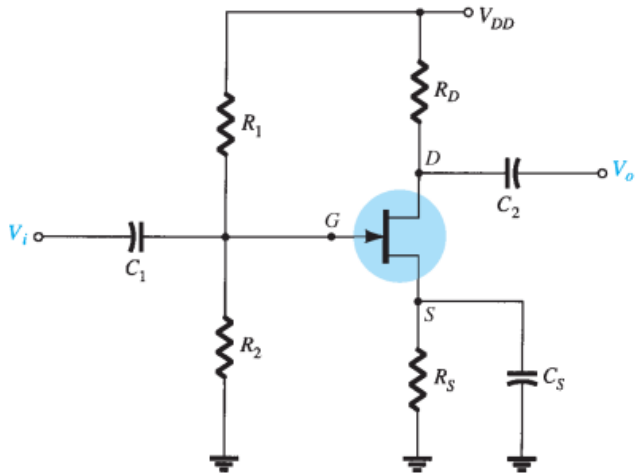
$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\ \text{mA}) R_S$$

$$V_{GS} = V_G|_{I_D = 0\ \text{mA}}$$

$$V_{GS} = V_G - I_D R_S$$
$$0\ \text{V} = V_G - I_D R_S$$

$$I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS} = 0\ \text{V}}$$



$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

Example

EXAMPLE 7.4 Determine the following for the network of Fig. 7.21:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

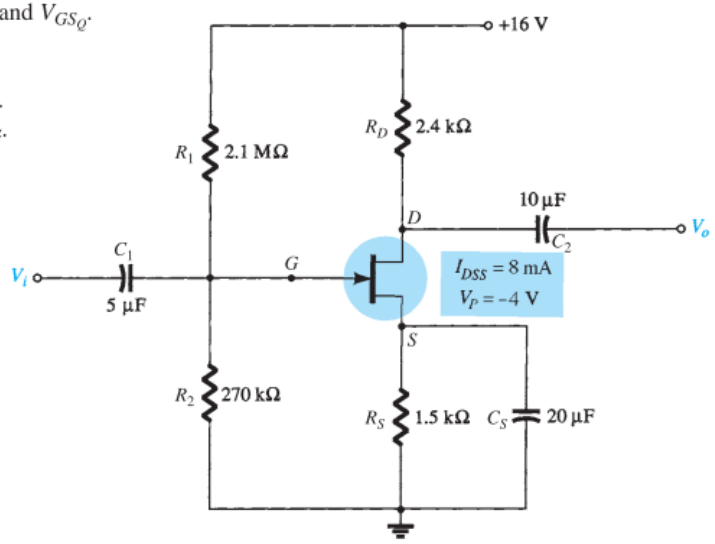


FIG. 7.21
Example 7.4.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega} = 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S = 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

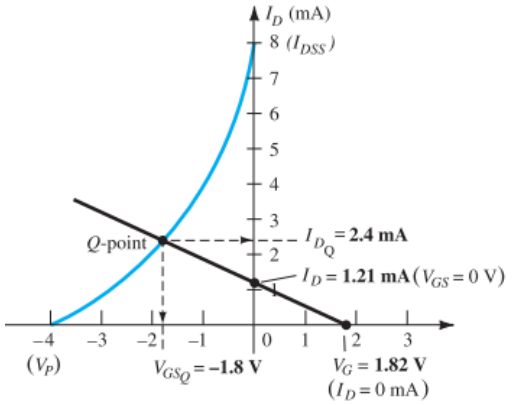


FIG. 7.22
Determining the Q-point for the network of Fig. 7.21.

When $I_D = 0\text{ mA}$,

$$V_{GS} = +1.82\text{ V}$$

When $V_{GS} = 0\text{ V}$,

$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$
$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$
$= \mathbf{10.24\text{ V}}$

c. $V_S = I_D R_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$
$= \mathbf{3.6\text{ V}}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$
$= \mathbf{6.64\text{ V}}$
or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$
$= \mathbf{6.64\text{ V}}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G = 10.24\text{ V} - 1.82\text{ V} = \mathbf{8.42\text{ V}}$$

DESIGN AND TROUBLESHOOTING

Design Example

EXAMPLE 7.14 For the network of Fig. 7.51, the levels of V_{D_Q} and I_{D_Q} are specified. Determine the required values of R_D and R_S. What are the closest standard commercial values?

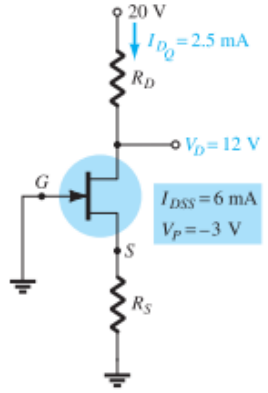


FIG. 7.51
Example 7.14.

$$R_{\text{unknown}} = \frac{V_R}{I_R}$$

Solution: As defined by Eq. (7.42),

$$R_D = \frac{V_{R_D}}{I_{D_Q}} = \frac{V_{DD} - V_{D_Q}}{I_{D_Q}}$$

and

$$= \frac{20\text{ V} - 12\text{ V}}{2.5\text{ mA}} = \frac{8\text{ V}}{2.5\text{ mA}} = \mathbf{3.2\,k\Omega}$$

Plotting the transfer curve in Fig. 7.52 and drawing a horizontal line at $I_{D_Q} = 2.5$ mA results in $V_{GS_Q} = -1$ V, and applying $V_{GS} = -I_D R_S$ establishes the level of R_S:

$$R_S = \frac{-(V_{GS_Q})}{I_{D_Q}} = \frac{-(-1\text{ V})}{2.5\text{ mA}} = \mathbf{0.4\,k\Omega}$$

The nearest standard commercial values are

$$R_D = 3.2\,\text{k}\Omega \Rightarrow \mathbf{3.3\,k\Omega}$$
$$R_S = 0.4\,\text{k}\Omega \Rightarrow \mathbf{0.39\,k\Omega}$$

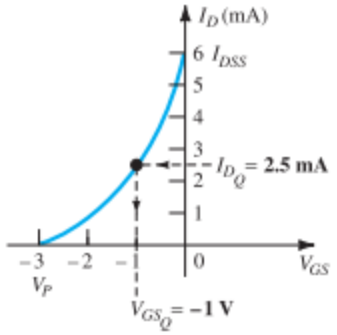


FIG. 7.52
Determining V_{GS_Q} for the network of Fig. 7.51.

Troubleshooting

The level of V_{DS} is typically between 25% and 75% of V_{DD} .

The continuity of a network can be checked simply by measuring the voltage across any resistor of the network.

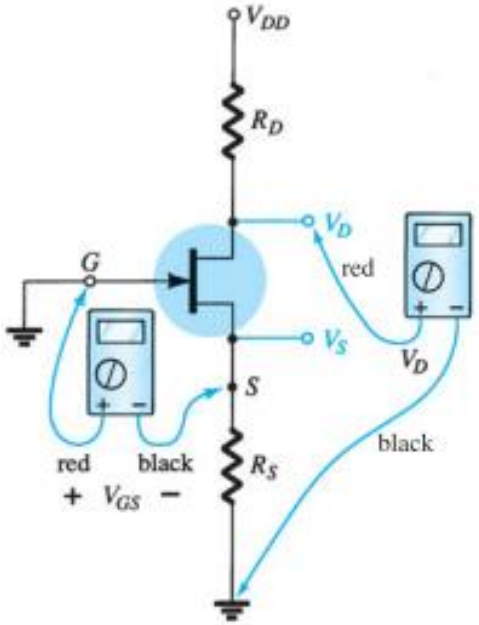
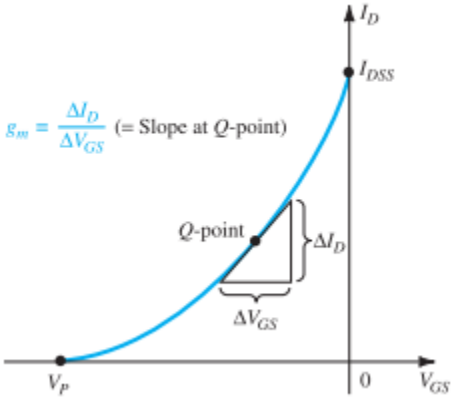


FIG. 7.55
Checking the dc operation of the JFET self-bias configuration.

JFET SMALL SIGNAL MODEL

JFET small signal Model

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$



$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

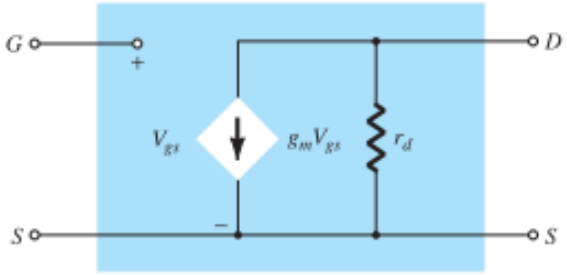


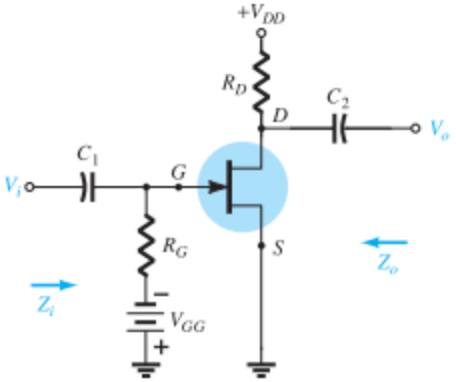
FIG. 8.8
JFET ac equivalent circuit.

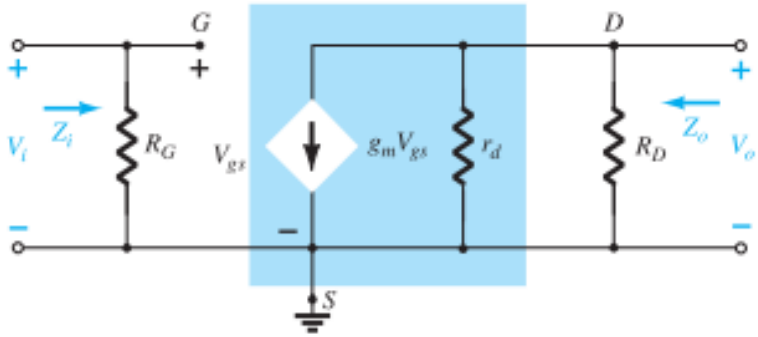
$$Z_i\,(\text{JFET}) = \infty\,\Omega$$

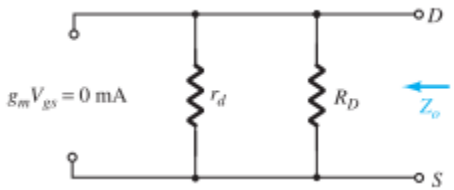
$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

Fixed-Bias Configuration







$$Z_i = R_G$$

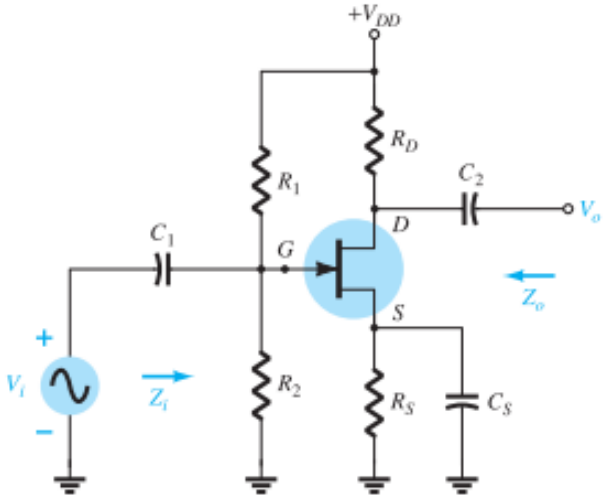
$$Z_o = R_D \| r_d \qquad Z_o \cong R_D \quad r_d \geq 10R_D$$

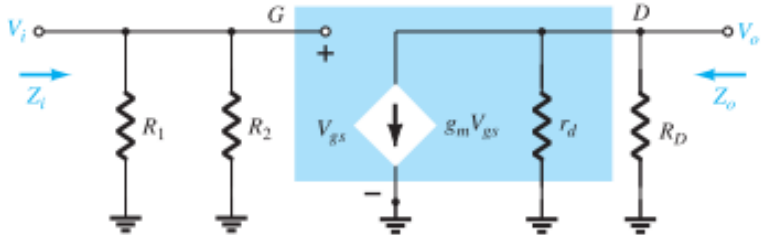
$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D$$

phase shift of 180° between input and output voltages.

VOLTAGE-DIVIDER CONFIGURATION





$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \qquad r_d \geq 10R_D$$

FET AMPLIFIER NETWORKS

Design FET Amplifier Network

EXAMPLE 8.14 Choose the values of R_D and R_S for the network of Fig. 8.44 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

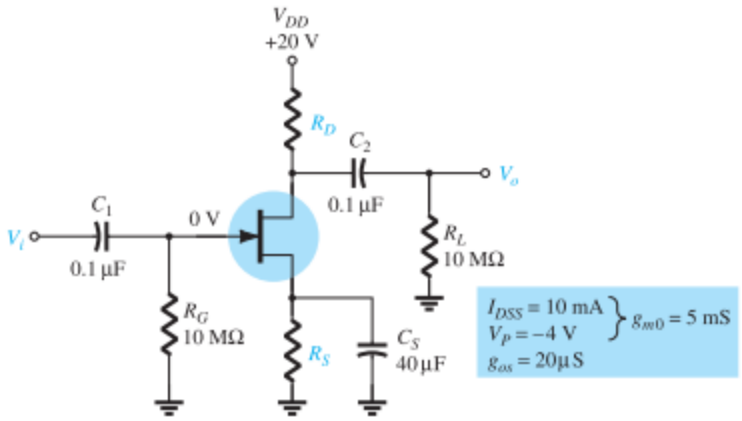


FIG. 8.44
Network for desired voltage gain in Example 8.14.

Solution: The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

and
$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

Determining g_m, we obtain

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$
$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values results in

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

so that
$$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{g_{os}} = \frac{1}{20\,\mu\text{S}} = 50\text{ k}\Omega$$

and
$$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

with the result that

$$R_D = \mathbf{2.2\text{ k}\Omega}$$

which is a standard value.

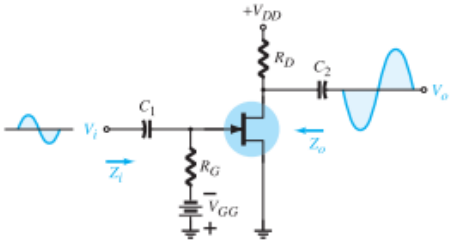
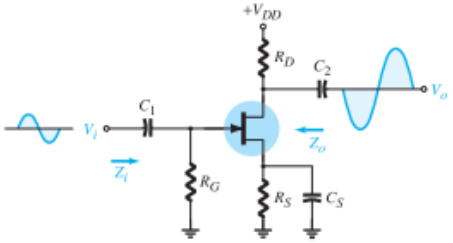
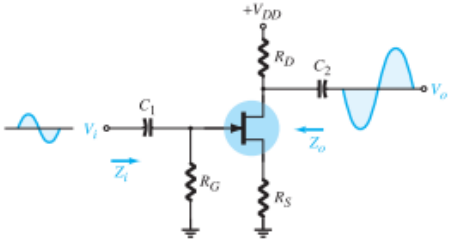
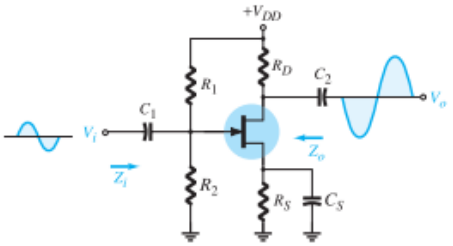
The level of R_S is determined by the dc operating conditions as follows:

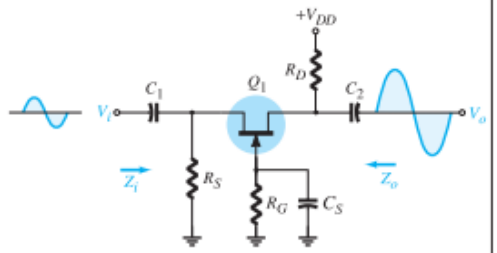
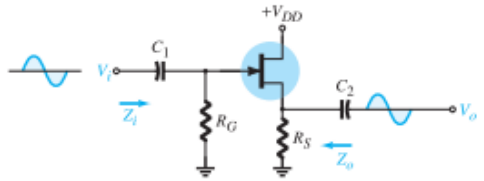
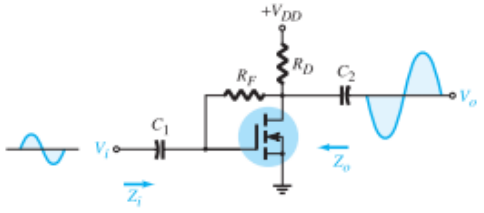
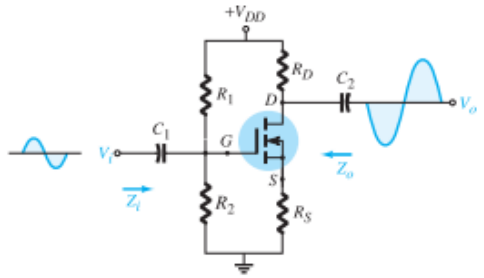
$$V_{GS_Q} = -I_D R_S$$
$$-1\text{ V} = -(5.625\text{ mA})R_S$$

and
$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is **180 Ω**. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

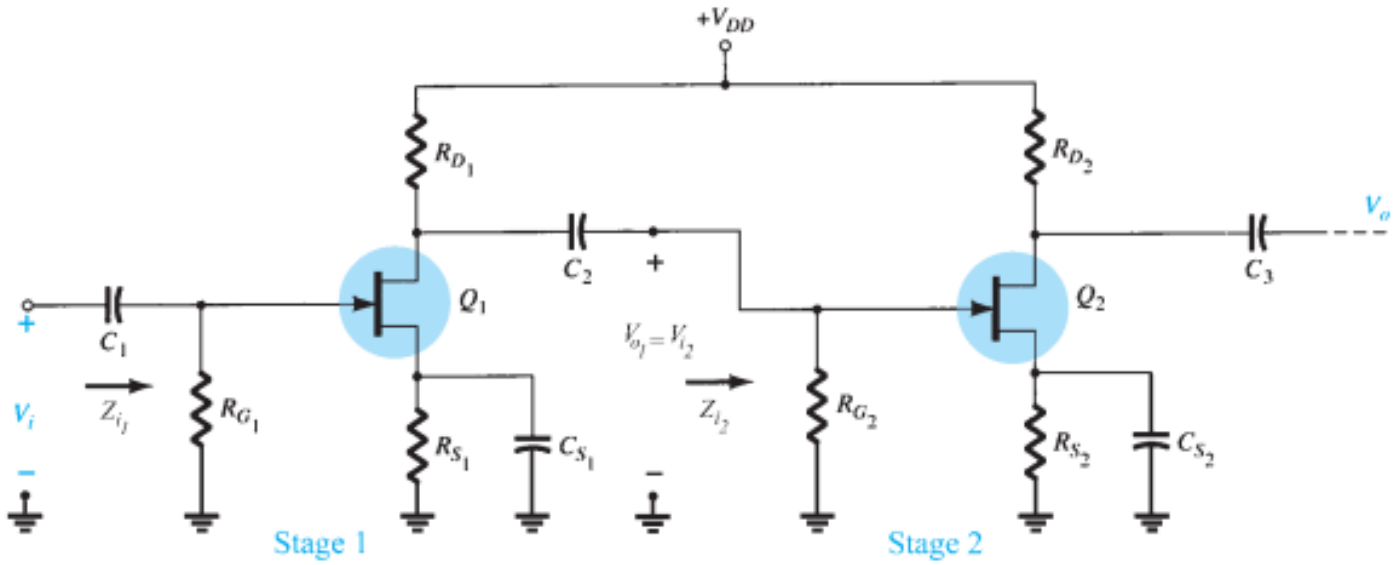
Summary Table

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $(r_d \geq 10R_D \text{ or } r_d = \infty\ \Omega)$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d} \right]$ $\cong R_S \| \frac{1}{g_m}$ $(r_d \geq 10 R_D)$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(R_d \geq 10 R_D)$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D$ $(r_d \geq 10 RD)$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m$ $(r_d \geq 10 R_S)$	Low (<1) $= \frac{g_m (r_d \| R_S)}{1 + g_m (r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10 R_S)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \frac{R_F + r_d \| R_D}{1 + g_m (r_d \| R_D)}$ $\cong \frac{R_F}{1 + g_m R_D}$ $(r_d \geq 10 R_D)$	Medium (2 kΩ) $= R_F \| r_d \| R_D$ $\cong R_D$ $(R_F, r_d \geq 10 R_D)$	Medium (−10) $= -g_m (R_F \| r_d \| R_D)$ $\cong -g_m R_D$ $(R_F, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10 R_D)$	Medium (−10) $= -g_m (r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10 R_D)$

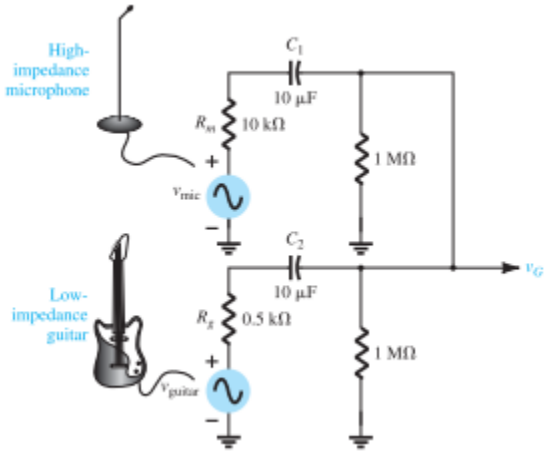
Cascaded Configuration

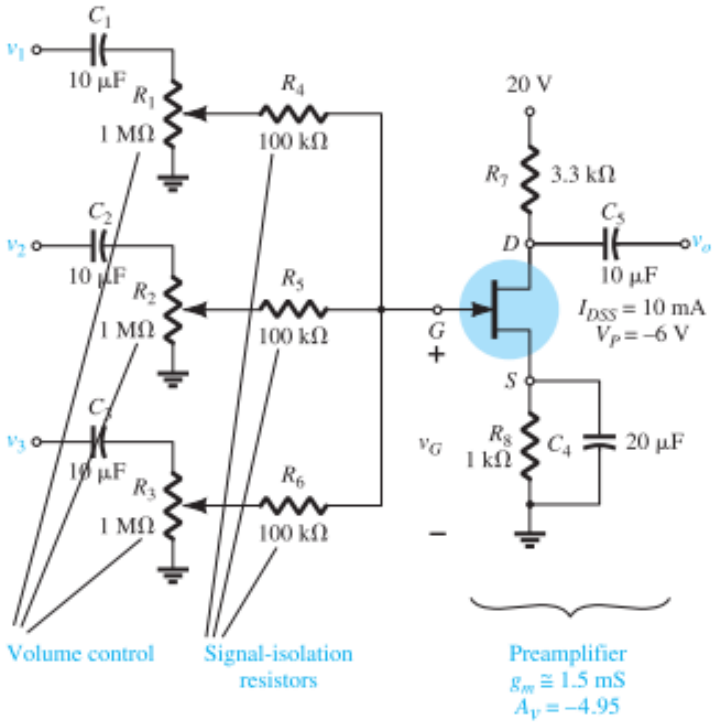
$$A_v = A_{v_1}A_{v_2} = (-g_{m_1}R_{D_1})(-g_{m_2}R_{D_2}) = g_{m_1}g_{m_2}R_{D_1}R_{D_2}$$



PRACTICAL APPLICATIONS

Three-Channel Audio Mixer





Motion Detection System

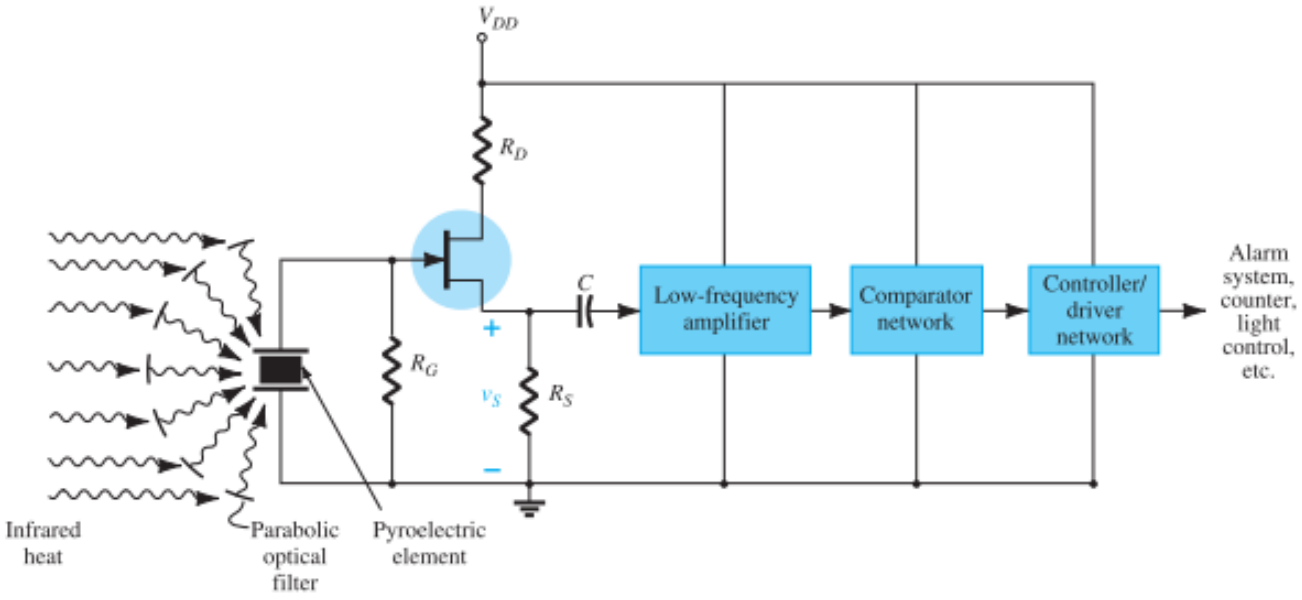


FIG. 8.59
Passive infrared (PIR) motion-detection system.

- For more details, refer to:
  - Chapter 6,7,8, Electronic Devices and Circuits, Boylestad.
- The lecture is available online at:
  - https://speakerdeck.com/ahmad_elbanna
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg